Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-12 (cancelled)

13 (previously presented): A network interface circuit for controlling data access of a network, the network interface circuit comprising:

a medium control module for transmitting a packet to the network, the medium control module comprising a buffer for storing the packet before transmission to the network;

a memory for temporarily storing a packet data corresponding to the packet before transmitting the packet data to the buffer, the memory including a check circuit; wherein in response to the memory transmitting the packet data to the buffer, the check circuit enables the memory to generate an interrupt request signal; and

a memory access circuit; wherein after receiving the interrupt request signal, the memory access circuit stores another packet data corresponding to another packet in the memory.

14 (previously presented): The network interface circuit of claim 13 wherein after the packet data is completely transmitted to the buffer, the check circuit sends the interrupt request signal.

15 (previously presented): The network interface circuit of claim 13 wherein when a portion of the packet is transmitted to the buffer, the check circuit sends the interrupt request signal for inputting a portion of another packet.

16 (cancelled)

17 (original): The network interface circuit of claim 13 wherein the operation of the memory is first-in-first-out.

18 (previously presented): The network interface circuit of claim 13 wherein the operation of the buffer is first-in-first-out.

19 (original): The network interface circuit of claim 13 wherein the network interface circuit is a full duplex network interface circuit.

20 (original): The network interface circuit of claim 13 wherein the memory controls all other memory units under a recycling memory unit operation.